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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
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EXAMINER	
DANG, PHUC T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,324	AHN ET AL.	
	Examiner	Art Unit	
	PHUC T DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-40 and 55-86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *73-77 and 82-86* is/are allowed.

6)☒ Claim(s) *33-38,40,55-59,61-70,72 and 78-81* is/are rejected.

7)☐ Claim(s) *39,60 and 71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4)☐ Interview Summary (PTO-413) Paper No(s) _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

1. This application is a divisional of U.S. Patent Application No. 09/514,629, filed on February 28, 2000.

Pre-Amendment

2. Pre-Amendment filed on August 30, 2001 has been entered and made of record as Paper No. 2.

In Pre-Amendment, applicant canceled claims 1-32 and 41-54, without prejudice or disclaimer, and new claims 55-86 were added. Claims 33-40 and 55-86 are now pending in the application.

Oath/Declaration

3. The new oath/declaration filed on August 30, 2001 is acceptable.

Information Disclosure Statement

4. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on August 30, 2001 and made of record as Paper No. 3.

Specification

5. The disclosure is objected to because of the following reasons:

Reference numeral "220A", "220B", "221A", "221B", "223A" and "223B" are not supported in Specification. Correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 33-34 are rejected under 35 U.S.C. 102 (b) as being anticipated by Okazawa (U.S. Patent No. 4,700,212).

Okazawa discloses the all features in the claimed invention, a semiconductor integrated circuit device includes a plurality of elements (col. 1, lines 9-29) such as a logic device and a memory device structure on a single substrate, comprising:

a first transistor for the logic device (110, Fig. 1) having a source (25, Fig. 1) and drain region (26, Fig. 1) includes a separated by a channel region (27, Fig. 1) in the substrate (21, Fig. 1), wherein the first transistor includes a dielectric layer (42, Fig. 3A) of a first thickness (Fig. 3A), including a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures (1000°C), separating a gate (28, 29, Fig. 1) from the channel region (27, Fig. 1); and

a second transistor for the memory device (210, Fig. 1) having a source (35, Fig. 1) and drain region (36, Fig. 1) in the substrate (21, Fig. 1) separated by a channel region (37, Fig. 1) in the substrate (21, Fig. 1), wherein the second transistor (210, Fig. 1) includes a dielectric layer (42, Fig. 3) of second thickness (fig. 3A) separating a gate (39, 38, Fig. 1) from the channel region (37, Fig. 1) [col. 5, lines 37-42].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 35-38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 33 above, and in view of Fang et al. (U.S. Patent No. 5,668,035) and in view of Liu et al. (U.S. Patent No.5,257,095) and in view of Cavin et al. (U.S. Patent No. 5,731,238) and in view of Lowrey et al. (U.S. Patent No. 5,057,449) and in view of Hasegawa (U.S. Patent No. 6,091,109).

Regarding claim 35, Okazawa discloses a logic device and memory device structure on a single substrate as discussed above but does not disclose the first transistor having a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers.

Liu, however, discloses the first transistor having a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers [col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the first transistor having a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometer for a purpose of requiring lower processing temperature.

Regarding claim 36, Okazawa discloses a logic device and memory device structure on a single substrate as discussed above but does not disclose the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4).

Cavins, however, discloses the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4) [Fig. 4 and col. 5, lines 58-64].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Cavins to Okazawa such that the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4) for a purpose of increasing the capacitance value of the integrated circuit device.

Regarding claim 37, Okazawa discloses a logic device and memory device structure on a single substrate as discussed above but does not disclose the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

Lowerey discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) [col. 3, lines 49-52].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey to Okazawa such that the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) for a purpose of improving electrical and physical characteristics over silicon dioxide.

Regarding claim 38, Okazawa discloses a logic device and memory device structure on a single substrate as discussed above but does not disclose the second transistor having a dielctric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

Hasegawa, however, discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa such that second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

8. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses a logic device and memory device structure on a single substrate, comprising:

a first transistor (110, Fig. 1), wherein the first transistor (110, Fig. 1) includes:

a first dielectric layer (42, Fig. 3A) of a first thickness (Fig. 3A);

a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures (1000°C); and a second transistor (210, Fig. 1), wherein the second transistor (210, Fig. 1) includes a second dielectric layer (43, Fig. 3A) of a second thickness (Fig. 3A) [col. 5, lines 37-42].

Okazawa does not close a first dielectric layer of a first thickness less than 5 nanometers.

Liu, however, discloses a first dielectric layer of a first thickness less than 5 nanometers [col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that a first dielectric layer of a first thickness less tan 5 nanometers for a purpose of requiring lower process temperature.

9. Claims 56 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 55 above, and in view of Liu et al. (U.S. Patent No. 5,257,095).

Regarding claim 56, Okazawa discloses the claimed invention as discussed above, but does not disclose the first dielectric layer and the top layer together have a thickness less than 7 nanometer.

Liu, however, discloses the first dielectric layer (150 Angstroms) and the top layer (5,500 Angstroms) together have a thickness less than 7 nanometer (5, 650 Angstroms) [col. 10, lines 66-col. 11, lines 4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the thickness of the first dielectric layer and the top layer together have a thickness less than 7 nanometer for a purpose of requiring lower processing temperature.

Regarding claim 61, Okazawa discloses the claimed invention as discussed above but does not disclose the top layer exhibits resistance to boron penetration at high temperature.

Liu, however, discloses the top layer exhibits resistance to boron penetration at high temperature [col. 10, lines 4-11].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the top layer exhibits resistance to boron penetration at high temperature for a purpose of providing for the reliable fabrication of an enhanced integrated circuit device.

10. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 55 above, and further in view of Cavins et al. (U.S. Patent No. 5,731,238).

Okazawa modified by Liu disclose the claimed invention as discussed above but does not disclose the first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

Cavins, however, discloses the first dielectric layer of a first thickness includes silicon dioxide and the top layer includes silicon nitride (col. 5, lines 58-64).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Cavins to Okazawa modified by Liu such that the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4) for a purpose of increasing the capacitance value of the integrated circuit device.

11. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 55 above, and further in view of Lowrey et al. (U.S. Patent No. 5,057,449).

Okazawa modified by Liu disclose the claimed invention as discussed above but does not disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

Lowrey discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) [col. 3, lines 49-52].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey to Okazawa modified by Liu such that the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) for a purpose of improving electrical and physical characteristics over silicon dioxide.

12. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 55 above, and further in view of Hasegawa (U.S. Patent No. 6,091,109).

Okazawa modified by Liu disclose the claimed invention as discussed above but does not disclose the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

Hasegawa, however, discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa modified by Liu such that second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

13. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses a logic device and memory device structure on a single substrate, comprising:

a first transistor (110, Fig. 1), wherein the first transistor (110, Fig. 1) includes:

a first dielectric layer (42, Fig. 3A) of a first thickness (Fig. 3A);

a top layer (43, Fig. 3A): and a second transistor (210, Fig. 1), wherein the second transistor (210, Fig. 1) includes a second dielectric layer (43, Fig. 3A) of a second thickness (Fig. 3A) [col. 5, lines 37-42].

Okazawa discloses the claimed invention as discussed above, but does not disclose a first dielectric layer of a first thickness less than 5 nanometers.

Liu, however, discloses a first dielectric layer of a first thickness less than 5 nanometers [col. 10, lines 63-col. 11, lines 4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that a first dielectric layer of a first thickness less than 5 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

14. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 62 above, and in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses the claimed invention as discussed above, but does not disclose the first dielectric layer and the top layer together have a thickness of less than 7 nanometers.

Hasegawa, however, discloses the first dielectric layer and the top layer together have a thickness of less than 7 nanometers [col. 10, lines 66-col. 11, lines 4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the first dielectric layer

and the top layer together have a thickness of less than 7 nanometers for a purpose of requiring lower process temperature.

15. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 62 above, and further in view of Hasegawa (U.S. Patent No. 6,091,109).

Okazawa modified by Liu disclose the claimed invention as discussed above, but does not disclose the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

Hasegawa, however, discloses the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa modified by Liu such that second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

16. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 62 above, and further in view of Cavins et al. (U.S. Patent No. 5,731,238).

Okazawa modified by Liu disclose the claimed invention as discussed above, but does not disclose the first dielectric layer of a first thickness includes silicon dioxide and the top layer includes silicon nitride.

Cavins, however, discloses the first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4) [col. 5, lines 58-64].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Cavins to Okazawa modified by Liu such that the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4) for a purpose of increasing the capacitance value of the integrated circuit device.

17. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 62 above, and further in view of Lowrey et al. (U.S. Patent No. 5,057,449).

Okazawa modified by Liu disclose the claimed invention as discussed above, but does not disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of siliocon dioxide.

Lowrey, however, discloses the second dielectric layer of a second thickness includes a dielectric layer formed entirely of siliocon dioxide (SiO_2) [col. 3, lines 39-42].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey to Okazawa modified by Liu such that the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) for a purpose of improving electrical and physical characteristics over silicon dioxide.

18. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses a logic device and memory device structure on a single substrate, comprising a first transistor (110, Fig. 1), wherein the first transistor (110, Fig. 1) includes:

a first dielectric layer (42, Fig. 3A) of a first thickness (Fig. 3A);

a silicon nitride (Si_3N_4) top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures; and a second transistor (210, Fig. 1), wherein the second transistor (210, Fig. 1) includes a second dielectric layer (43, Fig. 3A) of a second thickness (Fig. 3A) [col. 5, lines 37-42].

Okazawa discloses the claimed invention as discussed above, but does not disclose a first dielectric layer of a first thickness less than 5 nanometers.

Liu, however, discloses a first dielectric layer of a first thickness less than 5 nanometers [col. 10, lines 66-68].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that a first dielectric layer of a first thickness less than 5 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

19. Claims 68 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 67 above, and in view of Liu et al. (U.S. Patent No. 5,257,095).

Regarding claim 68, Okazawa discloses the claimed invention as discussed above, but does not disclose the first dielectric layer and the top layer together have a thickness of less than 7 nanometers.

Liu, however, discloses the first dielectric layer and the top layer together have a thickness of less than 7 nanometers [col. 10, lines 66-col. 11, lines4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the thickness of the first dielectric layer and the top layer together have a thickness less than 7 nanometer for a purpose of requiring lower processing temperature.

Regarding claim 72, Okazawa discloses the claimed invention as discussed above, but does not disclose a top layer exhibits a high resistance to boron penetration at high temperature.

Liu, however, discloses a top layer which exhibits a high resistance to boron penetration at high temperature [col. 10, lines 4-11].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the top layer exhibits resistance to boron penetration at high temperature for a purpose of providing for the reliable fabrication of an enhanced integrated circuit device.

20. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 67 above, and in view of Lowrey et al. (U.S. Patent No. 5,057,449).

Okazawa discloses the claimed invention as discussed above, but does not disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

Lowrey discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) [col. 3, lines 49-52].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey to Okazawa modified by Liu such that the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) for a purpose of improving electrical and physical characteristics over silicon dioxide.

21. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 67 above, and in view of Hasegawa (U.S. Patent No. 6,091,109).

Okazawa discloses the claimed invention as discussed above, but does not disclose the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

Hasegawa, however, discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers [col. 8, lines 31-33].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Hasegawa to Okazawa modified by Liu such that

second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

22. Claim 78 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095).

Okazawa discloses a logic device and memory device structure on a single substrate, comprising a first transistor (110, Fig. 1), wherein the first transistor (110, Fig. 1) includes:

a first dielectric layer (42, Fig. 3A) of a first thickness (Fig. 3A);

a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures; and a second transistor (210, Fig. 1), wherein the second transistor (210, Fig. 1) includes a second dielectric layer (43, Fig. 3A) of a second thickness (Fig. 3A) [col. 5, lines 37-42].

Okazawa discloses the claimed invention as discussed above, but does not disclose a first dielectric layer of a first thickness less than 5 nanometers and a second dielectric layer of a second dielectric layer of a second thickness less than 12 nanometers.

Liu, however, discloses a first dielectric layer of a first thickness less than 5 nanometers and a second dielectric layer of a second dielectric layer of a second thickness less than 12 nanometers [col. 10, lines 66-col. 11, lines 4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that a first dielectric layer of a first thickness less than 5 nanometers and a second dielectric layer of a second dielectric layer of

a second thickness less than 12 nanometers for a purpose of improving the desired characteristics and properties of the thickness of the gate oxide film.

23. Claims 79-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) as applied to claim 78 above, and in view of Liu et al. (U.S. Patent No. 5,257,095).

Regarding claim 79, Okazawa discloses the claimed invention as discussed above, but does not disclose a top layer exhibits a high resistance to boron penetration at high temperature.

Liu, however, discloses a top layer which exhibits a high resistance to boron penetration at high temperature [col. 10, lines 4-11].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the top layer exhibits resistance to boron penetration at high temperature for a purpose of providing for the reliable fabrication of an enhanced integrated circuit device.

Regarding claim 80, Okazawa discloses the claimed invention as discussed above, but does not disclose the first dielectric layer and the top layer together have a thickness of less than 7 nanometers.

Liu, however, discloses the first dielectric layer and the top layer together have a thickness of less than 7 nanometers [col. 10, lines 66-col. 11, lines4].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Liu to Okazawa such that the thickness of the first

dielectric layer and the top layer together have a thickness less than 7 nanometer for a purpose of requiring lower processing temperature.

24. Claim 81 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okazawa (U.S. Patent No. 4,700,212) in view of Liu et al. (U.S. Patent No. 5,257,095) as applied to claim 78 above, and further in view of Lowrey et al. (U.S. Patent No. 5,057,449).

Okazawa modified by Liu disclose the claimed invention as discussed above, but does not disclose the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

Lowrey discloses the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) [col. 3, lines 49-52].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Lowrey to Okazawa modified by Liu such that the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2) for a purpose of improving electrical and physical characteristics over silicon dioxide.

Allowable Subject Matter

25. Claims 39, 60 and 71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention. Okazawa (U.S. Patent No. 4,700,212), Hasegawa (U.S. Patent No. 6,091,109), Liu et al. (U.S. Patent No. 5,257,095),

Lowrey et al. (U.S. Patent No. 5,057,449) and Cavins et al. (U.S. Patent No. 5,731,238), taken individually or in combination, do not teach the claimed invention having a top layer of silicon nitride which comprises approximately a third of the first thickness of the dielectric layer.

26. Claims 73-77 and 82-86 were allowable over the prior art of record.

The following is a statement of reason for the indication of allowable subject matter:

Claims 73-77 and 82-86 are considered allowable since the prior art of record and the considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention. Okazawa (U.S. Patent No. 4,700,212), Hasegawa (U.S. Patent No. 6,091,109), Liu et al. (U.S. Patent No. 5,257,095), Lowrey et al. (U.S. Patent No. 5,057,449) and Cavins et al. (U.S. Patent No. 5,731,238), taken individually or in combination, do not teach the claimed invention having a top layer of silicon nitride of approximately a third of the first thickness, which exhibits a high resistance oxidation at high temperatures as disclosed in claims 73 and 82 and a pair of gate oxides thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers by krypton plasma generated atomic oxygen at approximately 400 degrees Celcius as disclosed in claim 86.

27. **THIS ACTION IS MADE FINAL**. Applicant is reminded of extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is field within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE MONTHS shortened statutory period, then the shortened statutory period willexpire on

the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a(will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Arguments

28. Applicant's arguments filed on 9/14/2000 have been fully considered but that are not persuasive and Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

29. In response to Applicant's arguments with respect to amended claims 1-4 and 6-8, clearly Okazawa (U. S. Patent No. 4,700,212) discloses all claimed subject matter as set forth in the last Office Action. In response to Applicant's contention Okazawa reference failed to teach a dielectric layer of a first thickness including a top layer which exhibits a high resistance to oxidation at high temperatures separating a gate from the channel region but Okazawa discloses the dielectric layer (42, Fig. 3A) or (29,39, Fig. 2A) including a top layer (43, Fig. 3A) or (28,38, Fig. 2A) separating a gate from the channel region (27, Fig. 2A) as recited in col. 5, lines 32-36.

In response to Applicant's contention Okazawa reference failed to show a logic device and a memory device structure on a single substrate, but Okazawa discloses a semiconductor integrated circuit device includes a plurality of elements (such as MOSFET's) as shown in col. 1, lines 15-18 beacause each element (integrated circuit device) has to have a logic device region and a memory device region on a single substrate.

Conclusion

30. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

31. A shortened statutory period for response to this Office action is set to expire 3 (three) months and 0 (zero) day from the date of this communication. Failure to response within the period for response will cause the application to become abandoned (see MPEP § 710.02(b)).

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 703-305-1080. The examiner can normally be reached on 8:00 am-5:00 pm.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

32. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Examiner

Art Unit 2818

David Nelms
Supervisory Patent Examiner
Technology Center 2800

December 9, 2002